**WE CLAIM:**

1. An electrically erasable and programmable zero-power memory cell comprising:

a first variable voltage generator;

a second variable voltage generator;

a P-channel sense transistor having a source coupled to said first variable voltage generator;

an N-channel sense transistor having a source coupled to said second variable voltage generator;

wherein a drain of said P-channel sense transistor is coupled to a drain of said N-channel sense transistor to form an output of the memory cell;

and wherein a gate of said P-channel sense transistor is coupled to a gate of said N-channel sense transistor to form a floating gate of the memory cell;

a write transistor having a source coupled to a WBL (write bit line) and having a gate coupled to a WL (write line);

a tunneling capacitor coupled between said floating gate of the memory cell and a drain of said write transistor; and

a coupling capacitor coupled between a CG (control gate) node and said floating gate of the memory cell;

wherein said CG (control gate) node is biased with a positive voltage during an erase operation and wherein said WBL (write bit line) and said WL (write line) are biased to turn on said write transistor such that a negative voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said P-channel sense transistor for forming a logical high state at said output of said memory cell during said erase operation;

and wherein said CG (control gate) node is biased with a ground or negative voltage during a program operation and wherein said WBL (write bit line) and said

WL (write line) are biased to turn on said write transistor such that a positive voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said N-channel sense transistor for forming a logical low state at said output of said memory cell during said program operation;

and wherein each of said first and second variable voltage generators applies a positive voltage at said respective source of each of said P-channel and N-channel sense transistors during said erase operation.

2. The electrically erasable and programmable zero-power memory cell of claim 1, wherein each of said first and second variable voltage generators applies a ground or negative voltage at said respective source of each of said P-channel and N-channel sense transistors during said program operation.

3. The electrically erasable and programmable zero-power memory cell of claim 1, wherein said P-channel sense transistor is comprised of a PMOSFET (P-channel metal oxide semiconductor field effect transistor), and wherein said N-channel sense transistor and said write transistor are comprised of NMOSFETs (N-channel metal oxide semiconductor field effect transistors).

4. The electrically erasable and programmable zero-power memory cell of claim 1, wherein a magnitude of the respective threshold voltage of each of said P-channel and N-channel sense transistors is higher than a magnitude of a threshold voltage of standard process P-channel and N-channel transistors.

5. The electrically erasable and programmable zero-power memory cell of claim 4, wherein a sum of a magnitude of a respective threshold voltage of said P-channel sense transistor and a magnitude of a respective threshold voltage of said N-channel sense

transistor is greater than a minimum value in a range of a difference of a first voltage generated by said first voltage generator and a second voltage generated by said second voltage generator during a read operation of said memory cell.

6. The electrically erasable and programmable zero-power memory cell of claim 4, wherein said magnitude of the respective threshold voltage of each of said P-channel and N-channel sense transistors is adjusted with a thickness of a respective gate oxide and with a concentration of respective channel doping for each of said P-channel and N-channel sense transistors.

7. The electrically erasable and programmable zero-power memory cell of claim 6, wherein the thickness of the respective gate oxide for each of said P-channel and N-channel sense transistors is for a high voltage MOSFET, and wherein the concentration of the respective channel doping for each of said P-channel and N-channel sense transistors is for a low voltage MOSFET.

8. The electrically erasable and programmable zero-power memory cell of claim 1, wherein said first variable voltage generator applies a positive voltage on said source of said P-channel sense transistor and applies a ground or negative voltage on said source of said N-channel sense transistor, during a read operation.

9. An electrically erasable and programmable zero-power memory cell comprising:

a first variable voltage generator;

a second variable voltage generator;

a P-channel sense transistor having a source coupled to said first variable voltage generator;

an N-channel sense transistor having a source coupled to said second variable voltage generator;

wherein a drain of said P-channel sense transistor is coupled to a drain of said N-channel sense transistor to form an output of the memory cell;

and wherein a gate of said P-channel sense transistor is coupled to a gate of said N-channel sense transistor to form a floating gate of the memory cell;

a write transistor having a source coupled to a WBL (write bit line) and having a gate coupled to a WL (write line);

a tunneling capacitor coupled between said floating gate of the memory cell and a drain of said write transistor; and

a coupling capacitor coupled between a CG (control gate) node and said floating gate of the memory cell;

wherein said CG (control gate) node is biased with a positive voltage during an erase operation and wherein said WBL (write bit line) and said WL (write line) are biased to turn on said write transistor such that a negative voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said P-channel sense transistor for forming a logical high state at said output of said memory cell during said erase operation;

and wherein said CG (control gate) node is biased with a ground or negative voltage during a program operation and wherein said WBL (write bit line) and said WL (write line) are biased to turn on said write transistor such that a positive voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said N-channel sense transistor for forming a logical low state at said output of said memory cell during said program operation;

and wherein each of said first and second variable voltage generators applies a ground or negative voltage at said respective source of each of said P-channel and N-channel sense transistors during said program operation.

10. An electrically erasable and programmable zero-power memory cell comprising:

a P-channel sense transistor having a source coupled to a first voltage generator;

an N-channel sense transistor having a source coupled to a second voltage generator;

wherein a drain of said P-channel sense transistor is coupled to a drain of said N-channel sense transistor to form an output of the memory cell;

and wherein a gate of said P-channel sense transistor is coupled to a gate of said N-channel sense transistor to form a floating gate of the memory cell;

a write transistor having a source coupled to a WBL (write bit line) and having a gate coupled to a WL (write line);

a tunneling capacitor coupled between said floating gate of the memory cell and a drain of said write transistor; and

a coupling capacitor coupled between a CG (control gate) node and said floating gate of the memory cell;

wherein said CG (control gate) node is biased with a positive voltage during an erase operation and wherein said WBL (write bit line) and said WL (write line) are biased to turn on said write transistor such that a negative voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said P-channel sense transistor for forming a logical high state at said output of said memory cell during said erase operation;

and wherein said CG (control gate) node is biased with a ground or negative voltage during a program operation and wherein said WBL (write bit line) and said WL (write line) are biased to turn on said write transistor such that a positive voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said N-channel sense transistor for forming a logical

low state at said output of said memory cell during said program operation;

and wherein a magnitude of the respective threshold voltage of each of said P-channel and N-channel sense transistors is higher than a magnitude of a threshold voltage of standard process P-channel and N-channel transistors.

11. The electrically erasable and programmable zero-power memory cell of claim 10, wherein a sum of a magnitude of a respective threshold voltage of said P-channel sense transistor and a magnitude of a respective threshold voltage of said N-channel sense transistor is greater than a minimum value in a range of a difference of a first voltage generated by said first voltage generator and a second voltage generated by said second voltage generator during a read operation of the memory cell.

12. The electrically erasable and programmable zero-power memory cell of claim 10, wherein the thickness of the respective gate oxide for each of said P-channel and N-channel sense transistors is for a high voltage MOSFET, and wherein the concentration of the respective channel doping for each of said P-channel and N-channel sense transistors is for a low voltage MOSFET.

13. An electrically erasable and programmable zero-power memory cell comprising:

a first variable voltage generator;

a second variable voltage generator;

a P-channel sense transistor having a source coupled to said first variable voltage generator;

an N-channel sense transistor having a source coupled to said second variable voltage generator;

wherein a drain of said P-channel sense transistor is coupled to a drain of said

N-channel sense transistor to form an output of the memory cell;

and wherein a gate of said P-channel sense transistor is coupled to a gate of said N-channel sense transistor to form a floating gate of the memory cell;

means for forming a negative voltage on said floating gate of the memory cell to turn on said P-channel sense transistor for forming a logical high state at said output of said memory cell during an erase operation;

means for forming a positive voltage on said floating gate of the memory cell to turn on said N-channel sense transistor for forming a logical low state at said output of said memory cell during a program operation;

wherein each of said first and second variable voltage generators applies a positive voltage at said respective source of each of said P-channel and N-channel sense transistors during said erase operation.

14. The electrically erasable and programmable zero-power memory cell of claim 13, wherein each of said first and second variable voltage generators applies a ground or negative voltage at said respective source of each of said P-channel and N-channel sense transistors during said program operation.

15. An electrically erasable and programmable zero-power memory cell comprising:

a first variable voltage generator;

a second variable voltage generator;

a P-channel sense transistor having a source coupled to said first variable voltage generator;

an N-channel sense transistor having a source coupled to said second variable voltage generator;

wherein a drain of said P-channel sense transistor is coupled to a drain of said

N-channel sense transistor to form an output of the memory cell;

and wherein a gate of said P-channel sense transistor is coupled to a gate of said N-channel sense transistor to form a floating gate of the memory cell;

means for forming a negative voltage on said floating gate of the memory cell to turn on said P-channel sense transistor for forming a logical high state at said output of said memory cell during an erase operation;

means for forming a positive voltage on said floating gate of the memory cell to turn on said N-channel sense transistor for forming a logical low state at said output of said memory cell during a program operation;

wherein a magnitude of the respective threshold voltage of each of said P-channel and N-channel sense transistors is higher than a magnitude of a threshold voltage of standard process P-channel and N-channel transistors.

16. The electrically erasable and programmable zero-power memory cell of claim 15, wherein a sum of a magnitude of a respective threshold voltage of said P-channel sense transistor and a magnitude of a respective threshold voltage of said N-channel sense transistor is greater than a minimum value in a range of a difference of a first voltage generated by said first voltage generator and a second voltage generated by said second voltage generator during a read operation of the memory cell.

17. The electrically erasable and programmable zero-power memory cell of claim 15, wherein the thickness of the respective gate oxide for each of said P-channel and N-channel sense transistors is for a high voltage MOSFET, and wherein the concentration of the respective channel doping for each of said P-channel and N-channel sense transistors is for a low voltage MOSFET.

18. A method for erasing and programming an electrically erasable and

programmable zero-power memory cell, the method comprising:

applying a first voltage generated by a first variable voltage generator on a source of a P-channel sense transistor;

applying a second voltage generated by a second variable voltage generator on a source of an N-channel sense transistor;

wherein a drain of said P-channel sense transistor is coupled to a drain of said N-channel sense transistor to form an output of the memory cell;

and wherein a gate of said P-channel sense transistor is coupled to a gate of said N-channel sense transistor to form a floating gate of the memory cell;

and wherein a write transistor has a source coupled to a WBL (write bit line), and has a gate coupled to a WL (write line), and has a drain coupled to said floating gate of the memory cell via a tunneling capacitor;

and wherein a coupling capacitor is coupled between a CG (control gate) node and said floating gate of the memory cell;

biasing said CG (control gate) node with a positive voltage during an erase operation and biasing said WBL (write bit line) and said WL (write line) to turn on said write transistor such that a negative voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said P-channel sense transistor for forming a logical high state at said output of said memory cell during said erase operation;

biasing said CG (control gate) node with a ground or negative voltage during a program operation and biasing said WBL (write bit line) and said WL (write line) to turn on said write transistor such that a positive voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said N-channel sense transistor for forming a logical low state at said output of said memory cell during said program operation; and

applying a positive voltage at said respective source of each of said P-channel

and N-channel sense transistors with said first and second variable voltage generators, during said erase operation.

19. The method of claim 18, further comprising:

applying a ground or negative voltage at said respective source of each of said P-channel and N-channel sense transistors with said first and second variable voltage generators, during said program operation.

20. The method of claim 18, wherein said P-channel sense transistor is comprised of a PMOSFET (P-channel metal oxide semiconductor field effect transistor), and wherein said N-channel sense transistor and said write transistor are comprised of NMOSFETs (N-channel metal oxide semiconductor field effect transistors).

21. The method of claim 18, wherein a magnitude of the respective threshold voltage of each of said P-channel and N-channel sense transistors is higher than a magnitude of a threshold voltage of standard process P-channel and N-channel transistors.

22. The method of claim 21, wherein a sum of a magnitude of a respective threshold voltage of said P-channel sense transistor and a magnitude of a respective threshold voltage of said N-channel sense transistor is greater than a minimum value in a range of a difference of a first voltage generated by said first variable voltage generator and a second voltage generated by said second variable voltage generator during a read operation of said memory cell.

23. The method of claim 22, wherein said magnitude of the respective threshold voltage of each of said P-channel and N-channel sense transistors is adjusted with a thickness of a respective gate oxide and with a concentration of respective channel doping for each of

said P-channel and N-channel sense transistors.

24. The method of claim 23, wherein the thickness of the respective gate oxide for each of said P-channel and N-channel sense transistors is for a high voltage MOSFET, and wherein the concentration of the respective channel doping for each of said P-channel and N-channel sense transistors is for a low voltage MOSFET.

25. The method of claim 18, further comprising:

applying a positive voltage on said source of said P-channel sense transistor with said first variable voltage generator and applying a ground or negative voltage on said source of said N-channel sense transistor with said second variable voltage generator, during a read operation.

26. A method for erasing and programming an electrically erasable and programmable zero-power memory cell, the method comprising:

applying a first voltage generated by a first variable voltage generator on a source of a P-channel sense transistor;

applying a second voltage generated by a second variable voltage generator on a source of an N-channel sense transistor;

wherein a drain of said P-channel sense transistor is coupled to a drain of said N-channel sense transistor to form an output of the memory cell;

and wherein a gate of said P-channel sense transistor is coupled to a gate of said N-channel sense transistor to form a floating gate of the memory cell;

and wherein a write transistor has a source coupled to a WBL (write bit line), and has a gate coupled to a WL (write line), and has a drain coupled to said floating gate of the memory cell via a tunneling capacitor;

and wherein a coupling capacitor is coupled between a CG (control gate) node

and said floating gate of the memory cell;

biasing said CG (control gate) node with a positive voltage during an erase operation and biasing said WBL (write bit line) and said WL (write line) to turn on said write transistor such that a negative voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said P-channel sense transistor for forming a logical high state at said output of said memory cell during said erase operation;

biasing said CG (control gate) node with a ground or negative voltage during a program operation and biasing said WBL (write bit line) and said WL (write line) to turn on said write transistor such that a positive voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said N-channel sense transistor for forming a logical low state at said output of said memory cell during said program operation; and

applying a ground or negative voltage at said respective source of each of said P-channel and N-channel sense transistors with said first and second variable voltage generators, during said program operation.

27. A method for erasing and programming an electrically erasable and programmable zero-power memory cell, the method comprising:

applying a first voltage on a source of a P-channel sense transistor;

applying a second voltage on a source of an N-channel sense transistor;

wherein a drain of said P-channel sense transistor is coupled to a drain of said N-channel sense transistor to form an output of the memory cell;

and wherein a gate of said P-channel sense transistor is coupled to a gate of said N-channel sense transistor to form a floating gate of the memory cell;

and wherein a write transistor has a source coupled to a WBL (write bit line), and has a gate coupled to a WL (write line), and has a drain coupled to said floating

gate of the memory cell via a tunneling capacitor;

and wherein a coupling capacitor is coupled between a CG (control gate) node and said floating gate of the memory cell;

biasing said CG (control gate) node with a positive voltage during an erase operation and biasing said WBL (write bit line) and said WL (write line) to turn on said write transistor such that a negative voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said P-channel sense transistor for forming a logical high state at said output of said memory cell during said erase operation; and

biasing said CG (control gate) node with a ground or negative voltage during a program operation and biasing said WBL (write bit line) and said WL (write line) to turn on said write transistor such that a positive voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said N-channel sense transistor for forming a logical low state at said output of said memory cell during said program operation;

wherein a magnitude of the respective threshold voltage of each of said P-channel and N-channel sense transistors is higher than a magnitude of a threshold voltage of standard process P-channel and N-channel transistors.

28. The method of claim 27, wherein a sum of a magnitude of a respective threshold voltage of said P-channel sense transistor and a magnitude of a respective threshold voltage of said N-channel sense transistor is greater than a minimum value in a range of a difference of a first voltage generated by said first voltage generator and a second voltage generated by said second voltage generator during a read operation of the memory cell.

29. The method of claim 27, wherein the thickness of the respective gate oxide for each of said P-channel and N-channel sense transistors is for a high voltage MOSFET, and

wherein the concentration of the respective channel doping for each of said P-channel and N-channel sense transistors is for a low voltage MOSFET.

30. A method for fabricating an electrically erasable and programmable zero-power memory cell, the method comprising:

forming a P-channel sense transistor having a source coupled to a first voltage generator;

forming an N-channel sense transistor having a source coupled to a second voltage generator;

wherein a drain of said P-channel sense transistor is coupled to a drain of said N-channel sense transistor to form an output of the memory cell;

and wherein a gate of said P-channel sense transistor is coupled to a gate of said N-channel sense transistor to form a floating gate of the memory cell;

performing a first channel doping implantation for implanting a P-type channel dopant into an N-channel region of said N-channel sense transistor,

wherein said a first concentration of said P-type channel dopant implanted into said N-channel region of said N-channel sense transistor is for a low voltage NMOSFET;

performing a second channel doping implantation for implanting an N-type channel dopant into a P-channel region of said P-channel sense transistor,

wherein said a second concentration of said N-type channel dopant implanted into said P-channel region of said P-channel sense transistor is for a low voltage PMOSFET;

forming an N-channel gate oxide over said N-channel region of said N-channel sense transistor;

wherein a first thickness of said N-channel gate oxide has a thickness of a gate oxide for a high voltage NMOSFET; and

forming a P-channel gate oxide over said P-channel region of said P-channel sense transistor;

wherein a second thickness of said P-channel gate oxide has a thickness of a gate oxide for a high voltage PMOSFET.

31. The method of claim 30, further comprising:

forming a write transistor having a source coupled to a WBL (write bit line) and having a gate coupled to a WL (write line);

forming a tunneling capacitor coupled between said floating gate of the memory cell and a drain of said write transistor; and

forming a coupling capacitor coupled between a CG (control gate) node and said floating gate of the memory cell;

wherein said CG (control gate) node is biased with a positive voltage during an erase operation and wherein said WBL (write bit line) and said WL (write line) are biased to turn on said write transistor such that a negative voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said P-channel sense transistor for forming a logical high state at said output of said memory cell during said erase operation;

and wherein said CG (control gate) node is biased with a ground or negative voltage during a program operation and wherein said WBL (write bit line) and said WL (write line) are biased to turn on said write transistor such that a positive voltage forms on said floating gate of the memory cell by charge tunneling through said tunneling capacitor to turn on said N-channel sense transistor for forming a logical low state at said output of said memory cell during said program operation.